SAC4015QP3

MMIC Low Noise Amplifier
5～18GHz

Rev 1.0

Features

- Frequency: 5~18GHz
- Gain: 20dB
- Noise Figure: 1.1dB Typ. 1.6dB Max.
- Output P_{-1}dB: 11dBm@+4V
- Supply Voltage: +3V/20mA, +4V/30mA
- Package Size: 3mmx3mmx0.75mm
- Die Size: 0.7mmx0.58mmx0.1mm

Typical Applications

- Telecommunication
- SATCOM

General Description

SAC4015QP3 is a MMIC Low Noise Amplifier die which operates between 5GHz~18GHz. The amplifier can provide 20dB gain, 11dBm OutputP_{-1}dB, 1.1dB noise figure from a 20mA supply current.

The bare chip offers full passivation for increased reliability and moisture protection. This amplifier is the perfect alternative to higher cost hybrid amplifiers.

Electrical Performance

T_A=25℃, V_D=+4V, I_D=30mA, Z_0=50Ω

Parameter	Min.	Typ.	Max.	Units
Frequency Range		5~13		GHz
Gain	18	20	25	dB
Gain Flatness	—	±1	±1.5	dB
Input/Output VSWR	—	1.3	1.8	:1
Noise Figure	—	1.1	1.6	dB
Reverse Isolation	—	-37	—	dB
Output Power for 1 dB Compression (OP$_{-1}$dB)	8	11	—	dBm
Output IP_3	—	23	—	dBm
Supply Current (I_D)	—	30	43	mA

Absolute Maximum Ratings

Maximum Input Power	+18dBm, CW 30s	Operating Temperature	-55℃~+85℃
Channel Temperature	+150℃	Storage Temperature	-55℃~+150℃
Working Voltage	+7V		

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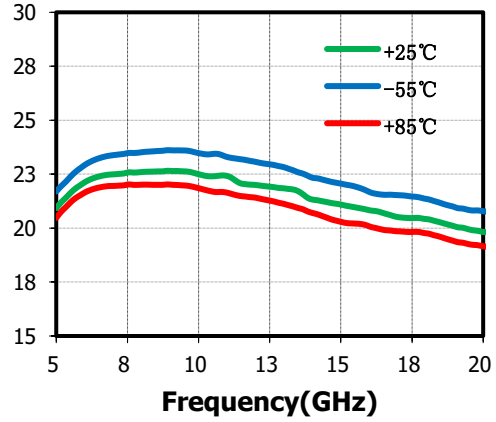
Typical Performance Curve

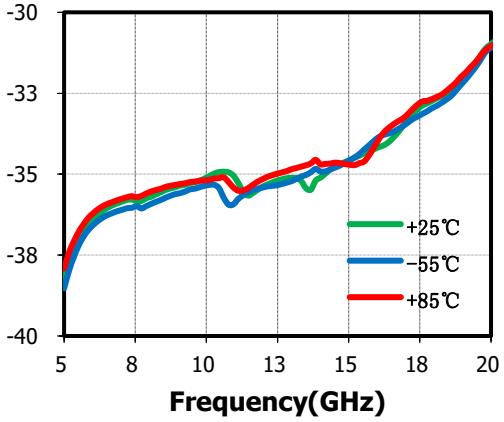
V_D=+4V, I_{DQ}=13mA, the following curves are taken from SAC4015QP3 evaluation board. De-embedding operation has been Implemented.

The noise coefficient (figure) is tested using the cold source method, and the calibration method is scalar calibration.

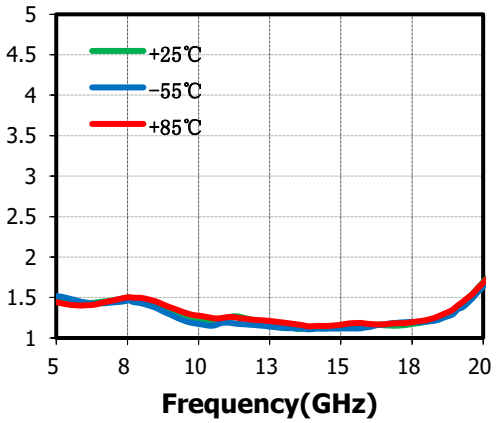
Small Signal Gain(dB) vs.Temperature



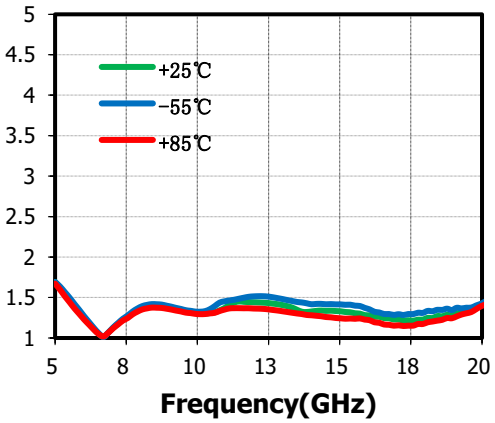
Reverse Isolation(dB) vs.Temperature



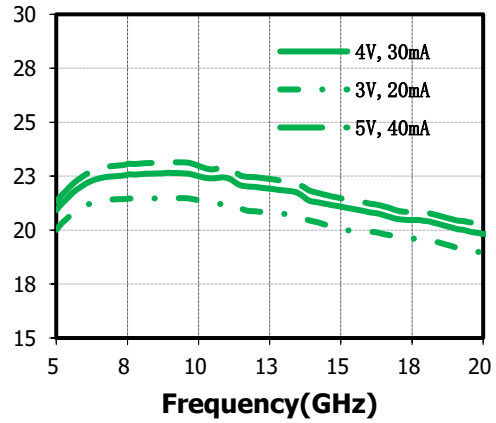
Input VSWR(:1) vs.Temperature



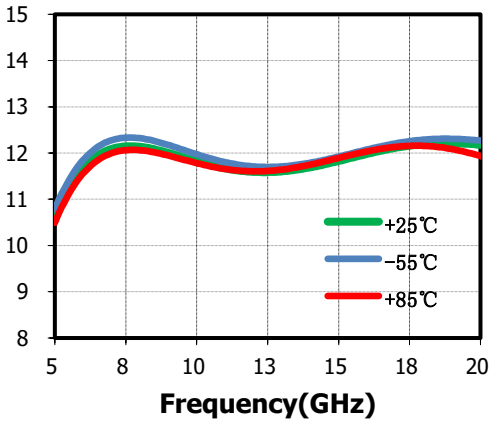
Output VSWR(:1) vs.Temperature



Small Signal Gain(dB) vs.VD



Output P-1dB(dBm) vs.Temperature



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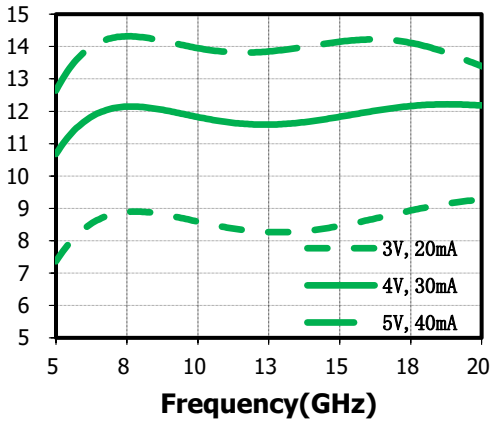
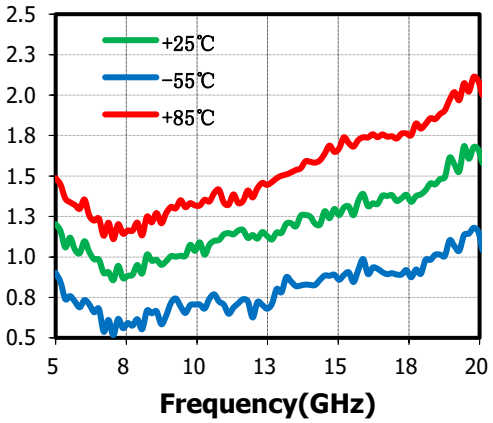
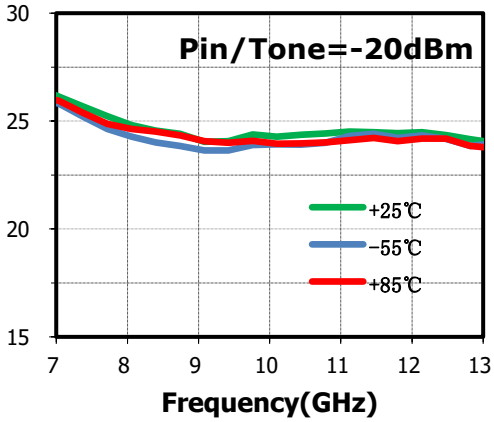
Output P-1dB(dBm) vs.VD



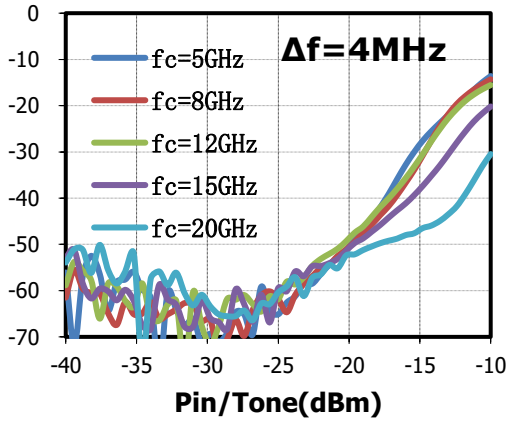
Noise Figure(dB) vs.Temperature



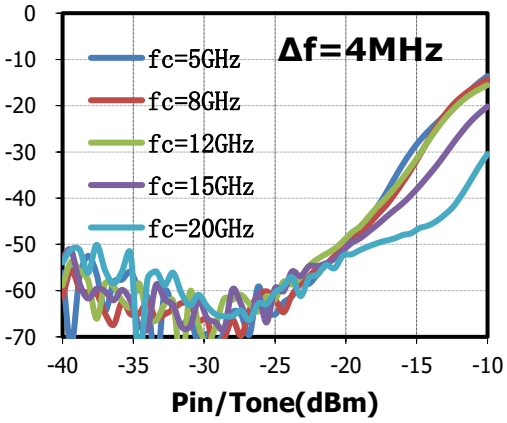
Output IP3(dBm) vs.Temperature



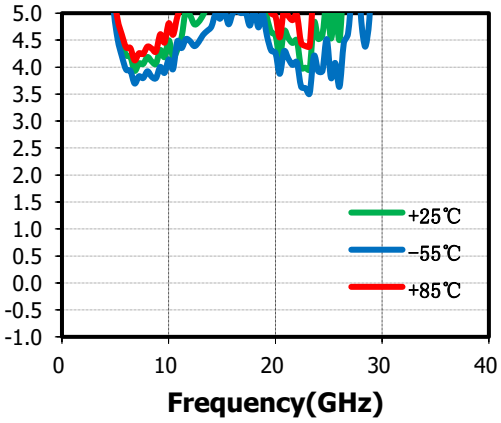
IM3(dBc)vs.Pin/Tone



IM5(dBc)vs.Pin/Tone



K factor(U) vs.Temperature



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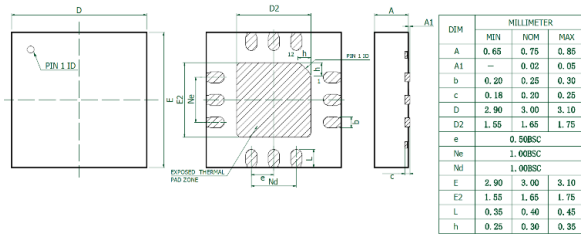
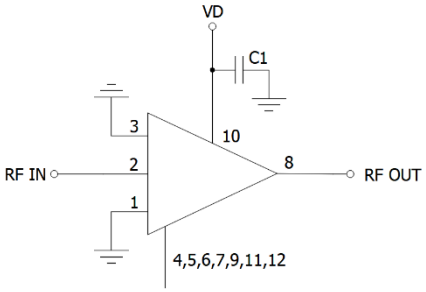
Outline Drawing

(All dimensions in mm)



DIM	MILLIMETER		
	MIN	NOM	MAX
A	0.65	0.75	0.85
A1	--	0.02	0.05
b	0.20	0.25	0.30
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D2	1.55	1.65	1.75
e	0.50BSC		
Ne	1.00BSC		
Nd	1.00BSC		
E	2.90	3.00	3.10
E2	1.55	1.65	1.75
L	0.35	0.40	0.45
h	0.25	0.30	0.35

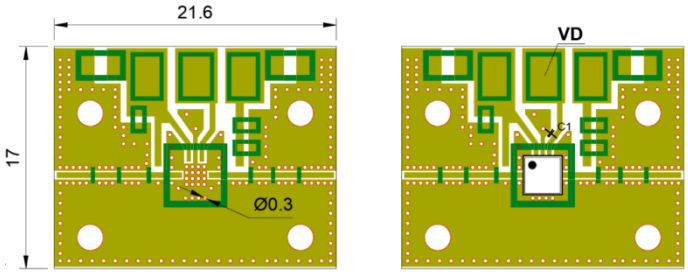
Assembly Diagram



Pin Function

Pin No.	Description	Pin No.	Description
1	Connect to ground	7	Connect to ground
2	RF input, DC Coupled	8	RF output, DC Coupled
3	Connect to ground	9	Connect to ground
4	Connect to ground	10	Drain supply
5	Connect to ground	11	NC or connect to ground
6	Connect to ground	12	NC or connect to ground

SAC4015QP3 Evaluation Board



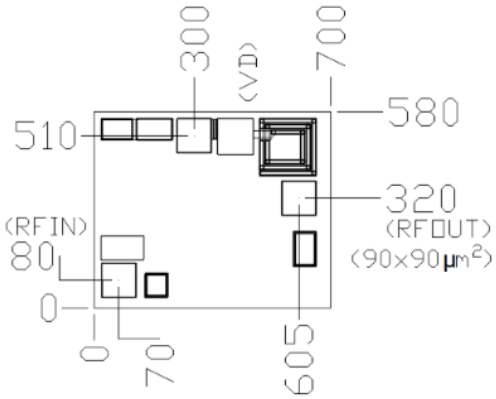
The Evaluation board is a 2-layer board fabricated using Rogers 4350 t=0.254 and using best practices for high frequency RF design. The RF input and RF output traces have a 50 Ω characteristic impedance.

Components List

Reference Des.	Value	Part Number	Manuf.
C1	0.01uF	GRM0336R61A103KE	Murata

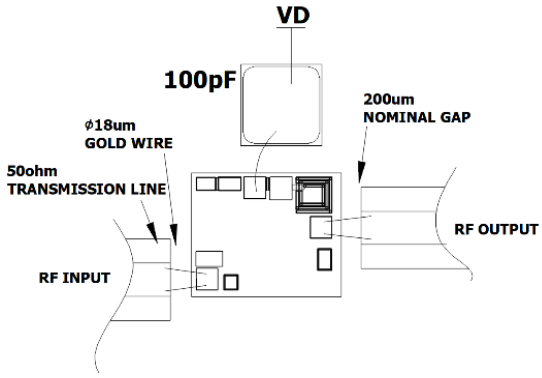
Die Outline Drawing

(All dimensions in μm)



t=100 μm

Assembly Diagram



Attention:

1. Bare chips need to be stored in a dry, nitrogen environment and used in an ultra-clean environment;

2. The chip should be sintered with conductive adhesive or alloy (the alloy temperature should not exceed 300 ℃, and the time should not exceed 30 seconds) to ensure sufficient grounding;

3. The gap between the chip microwave port and the substrate should not exceed 350μm Φ 18μm wire bonding, recommended wire length 250-350μm;

4. The RF input and output ports of the chip have integrated DC capacitors, with a withstand voltage of 15V;

5. The moisture proof level of the packaged product is Class 1a, and the storage environment is less than or equal to 30 ℃/60% RH, with a lifespan of four workshops;

6. When using packaged products, try to use thin RF boards as much as possible and increase the number of groundings vias at the bottom of the device to reduce the grounding inductance;

7. Remove the vacuum packaging and bake in a 125+/-5°environment for 6 hours before reflow soldering.

Revision History

Revision	Date	Comment
1.0	August 2, 2023	First Release