

SAC5020CR10



GaN IMFET
0.7GHz~6GHz 48dBm

Rev 1.1

Features

- Frequency: 0.7GHz~6GHz
- Large Signal Gain: 8dB
- Output Power: 48dBm
- DE: 45%
- Package: Metal-Ceramic-Package (CR10)
- Supply Voltage: +28V/-Vg

Typical Applications

- EMC
- Radar

General Description

SAC5020CR10 is a broad band IMFET delivering 48dBm with 45% drain efficiency from 0.7GHz to 6GHz. No external matching is required to achieve 0.7 to 6GHz operation.

Electrical Performance

$T_{BASE}=23^{\circ}C, V_D=+28V, I_{DQ}=1.1A, Z_0=50\Omega, T_{BASE}=+30^{\circ}C, CW$

Parameter	Min.	Typ.	Max.	Units
Frequency Range	0.7	—	6	GHz
Large Signal Gain	—	8	—	dB
Reverse Isolation	—	24	—	dB
RF Input Port Return Loss	6	12	—	dB
Output Power	—	48	—	dBm
Drain Voltage (V_D)	—	28	—	V
Gate Current	—	—	26	mA
Supply Current (I_D)*	—	—	16	A

*Adjust Vg between -3V to -1.5V to achieve $I_{DQ}=1.1A$, and typical Vg voltage is -2.4V

Absolute Maximum Ratings

Maximum Input Power	+44dBm	Operating Temperature (T_{BASE})	-55°C~+85°C
Channel Temperature	230°C	Storage Temperature	-55°C~+180°C
Maximum V_D	+35V	V_G Range	-8V~-1 V
Mounting Temperature	280°C,30s		

SuperApex, LLC

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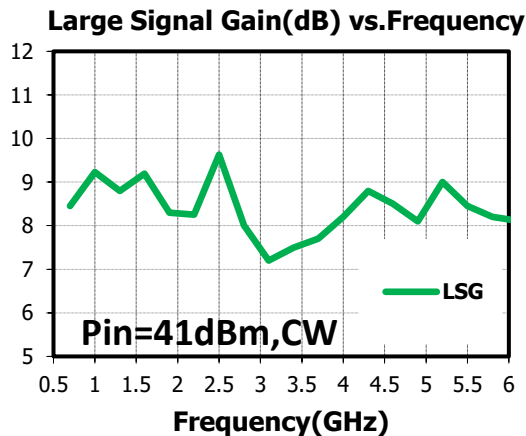
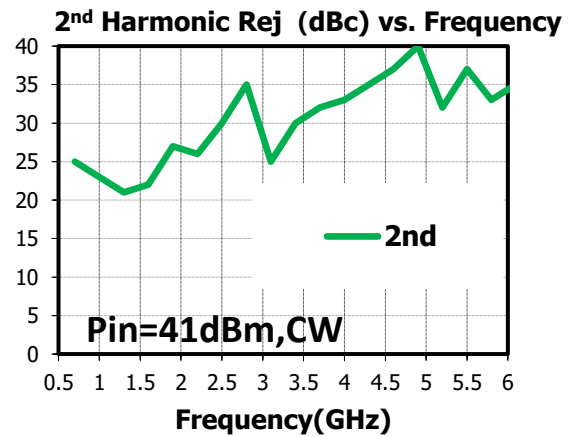
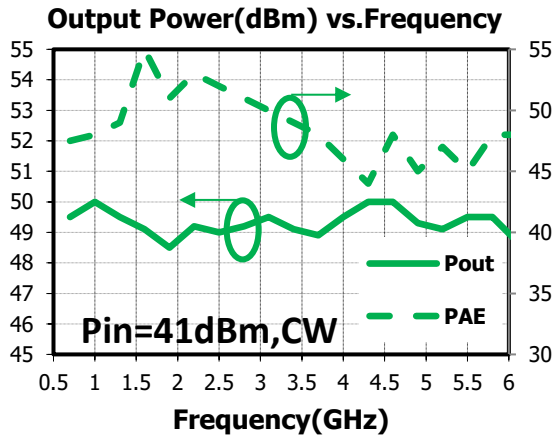


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Typical Performance Curve

The following curves are taken from SAC5020CR10 evaluation board. De-embedding operation has been implemented. $V_D=+28V$, $I_{DQ}=1.1A$, $T_{BASE}=+30^{\circ}C$, CW Operation



Thermal Resistance

Parameter	Conditions	Value	Unit
θ_{JC1}	$V_D=+28V$, $T_{BASE}=+70^{\circ}C$, $Pin=+41dBm$, CW, $f=6GHz$	1.12	$^{\circ}C/W$

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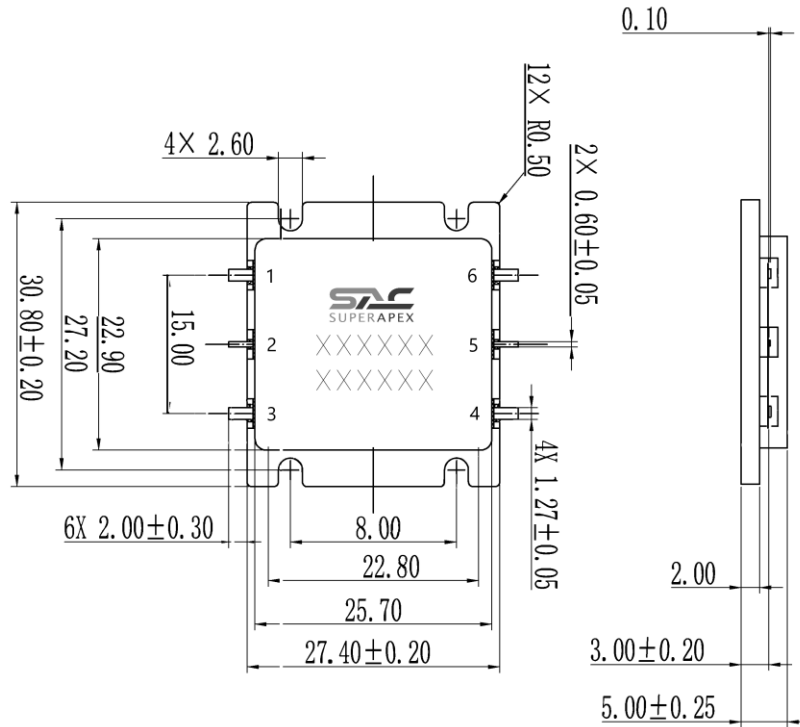


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Outline Drawing

(All dimensions in mm)



Pin Descriptions

Pin No.	Function	Pin No.	Function
1	Gate	4	Drain
2	RF input, AC Coupled	5	RF Output, AC Coupled
3	Gate	6	Drain

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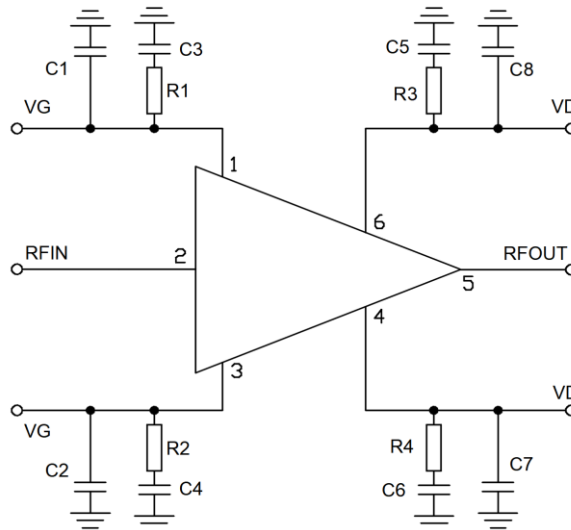
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Application Circuit



BOM

Reference Des.	Value	Part Number	Manuf.	Size
C1, C2	0.47 μ F	—	—	0805
C3~C6	0.022 μ F	—	—	0805
C7, C8	0.22 μ F	—	—	0805
R1~R8	2.2 Ω	—	—	0805

Notes

- SAC5020CR10 requires VDx and VGx bias.
Turn-on: Apply VGx, Apply VDx, Apply RFIN signal.
Turn-off: Remove RFIN signal, Decrease VG to -5V(pinch-off), Decrease VD to 0 V;
- The flange of package may be attached using screws, recommended torque for screw mounting is 10N-cm;
- The surface finish of the heat sink should be better than 0.8 μ m, and the surface flatness must be better than 10 μ m;
- Silicon based heat sink compounds should not be used for the thermal conductive grease. They cause poor grounding of the source flange. contamination and long-term degradation of thermal resistance between the FET package and heat sink;
- The chip is an Electrostatic Sensitive Device;
- The maximum soldering temperature for device pins is 400 °C/3s.

Revision History

Revision	Date	Comment
1.0	Dec. 13, 2024	First Release
1.1	Jan.2, 2025	Revise typo, Electrical Performance/ Frequency Range

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